



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Rajeev Balasubramonian, et al.

Appln. No.: 10/764,688

Filed: January 27, 2004

For: MEMORY HIERARCHY RECON-
FIGURATION FOR ENERGY AND
PERFORMANCE IN GENERAL-PURPOSE
PROCESSOR ARCHITECTURES

) Patent No.: 6,834,328 B2
) Issued: December 21, 2004
) Examiner: Anh K. Phung
) Art Unit: 2824
) Confirmation No.: 9448
) Date: March 11, 2005

SUBMISSION OF CERTIFICATE OF CORRECTION
UNDER 37 C.F.R. §1.323

**ATTENTION: Decision and Certificate of Correction
 Branch of the Patent Issue Division**

Commissioner for Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450

Sir:

The Patentees in the above-identified patent hereby submit a Certificate of Correction
 to correct error which was the fault of the Patentees.

03/16/2005 AWONDAF2 00000019 6834328

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Certificate
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 of Correction

A check for the requisite fee in the amount of \$100.00 is enclosed. However, if the attached fee proves to be insufficient, the Commissioner of Patents is authorized to charge any deficiency or credit any overpayment to Deposit Account No. 23-2185.

Respectfully submitted,

Sandhya Dwarkadas, et al..

By:

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 6,834,328 *B2*

DATED : December 21, 2004

INVENTOR(S) : Dwarkadas, et al.

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

COLUMN 1

Between lines 4 and 5 insert the following:

-- **Statement of Government Interest**

This work was supported in part by Air Force Research Laboratory Grant F296091-00-K-0182 and National Science Foundation Grants CCR9701915; CCR9702466; CCR9811929; CDA9401142; and EIA9972881. The government has certain rights in the invention.--

MAILING ADDRESS OF SENDER:

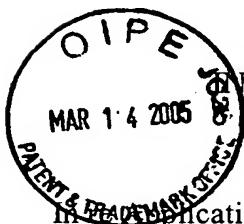
PATENT NO. 6,834,328

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Dec 23 2005



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TRADE MARK
specification of

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